Vimarsh Sathia

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EDUCATION

- **University of Illinois Urbana Champaign** *2022 – Present*
  Ph.D. in Computer Science. *Advised by Prof. Charith Mendis*
- **Indian Institute of Technology Madras** *2017 – 2021*
  B.Tech in Computer Science. GPA - 9.22/10

PUBLICATIONS

- **SENSEi: Input-Sensitive primitive compositions for GNN computations** *2024*
  Lenadora D., ***Sathia V.***, Georgiannis G., Yesil S., Torrellas J. and Mendis C. Under review
- **Accelerating Genetic Programming using GPUs** *2021*
  Sathia V., Ganesh V.*, and Thejaswi N.S.* preprint
  (* *Nvidia Corporation*)

RESEARCH AND PROJECTS

- **Using Program Synthesis to Optimize Vector Schedules in TACO** *Jan 2023 - May 2023*
  Advisor: Prof. Vikram Adve
  - Introduced a new backend to the Tensor Algebra Compiler(TACO) which uses program synthesis to perform auto-vectorization for `x86` backends.
  - Enables auto-generation and use of hardware specific vectorization and swizzle intrinsics without user intervention.

- **Using Evolutionary Computing for Mapspace Search in Timeloop** *Aug 2022 - Dec 2022*
  Advisor: Prof. Charith Mendis
  - Implemented genetic mapspace search in Timeloop - a simulator for DNN architectures.
  - Our algorithm achieves convergence within 4 iterations, which is way faster than the search strategies in Timeloop.

- **Optimizing Symbolic Regression on GPUs** *2021*
  Advisor: Prof. Rupesh Nasre & Collaborator: NVIDIA Corporation
  - Designed a GPU accelerated stack-based variant of the generational GP algorithm, achieving $40\times$ to $119\times$ speedups over existing frameworks.
  - Algorithm implementation merged into cuml, NVIDIA's open source suite of GPU-accelerated machine learning algorithms.

- **Improving Context Insensitive Escape Analysis** *2021*
  Advisor: Prof. Nandivada V. Krishna
  - Proposed optimizations for lock elision, which uses May Happen in Parallel(MHP) information to remove mutex synchronizations on *GlobalEscape* marked objects in Java.

INDUSTRIAL EXPERIENCE

- **Microsoft India** *2021 – 2022*
  Software Engineer, Azure for Operators
  - Added support for Lawful Interception in 5G telecommunication networks.
  - Reduced memory footprint of the core microservice by $3\times$ using de-duplication of UUIDs.

VOLUNTEERING

- **Organizer, UIUC Compiler Seminar (link)** *Feb 2023 – Dec 2023*
  Directed seminar with student presentations and invited speakers, promoting exposure to ongoing compiler research from reputable conferences.

ACADEMIC HONORS

- **Recipient, C S Krishnamoorthy Endowment Award** *June 2021*
  Awarded for the best thesis in the area of Genetic Algorithms and Evolutionary Computation amongst B.Tech and M.Tech projects